Abstract—The low frequency noise of nanoscale electrostatically gated FETs will determine the ISFET or BioFET sensor signal-to-noise ratio and is hence of key importance for FET-based biosensing applications. We report on the 1/f noise of fully integrated electrostatically gated FETs fabricated in a 300mm fabrication facility with fin widths down to 20nm. We observe a 1/f noise power spectral density (PSD) for a 20nm wide, 10µm long device down to ~1x10⁻⁹V²/Hz, which is significantly lower than previously reported for electrostatically gated top-down fabricated FETs. We find the gate referred noise PSD to increase with increasing overdrive, indicating that lower overdrive is better for sensor signal-to-noise ratio.

Keywords—ISFET, BioFET, FinFET, 1/f noise, pink noise

In this work the low frequency noise of electrostatically gated pMOS finFETs was characterized. The inversion mode pMOS finFET devices were fully fabricated in a 300mm processing facility in a process derived from a solid gate finFET process [1]. Fin width reached down to 20nm. These devices had a 4nm SiON gate dielectric. During gating the gate dielectric was exposed to a 15mM phosphate buffered saline (PBS) electrolyte solution contacted by means of a Ag/AgCl electrode.

The typical drain current vs. gate voltage characteristic (Iᵥ-Vᵥ) is shown in the inset of fig. 1. The gate voltage referred noise spectrum exhibits 1/f behavior (see fig. 1).

We have investigated the geometry dependence of the gate voltage referred noise power and find it to scale inversely proportional to length, as expected.

The gate bias dependence of the gate voltage referred noise power at 10Hz is shown in fig. 2 for 20nm finFET devices with length 1µm and 10µm. We observe that the noise power decreases with decreasing overdrive. This is in agreement with the findings of Kim et al. [2] who report the noise characteristics of 50nm wide top-down fabricated electrostatically gated nFETs, and who also observe increasing gate bias referred noise power at higher overdrive. This is also in agreement with the carbon nanotube work [4] and the theory in [5]. Rajan et al. [3], however, report a different gate bias dependence of noise power for 100nm wide top-down nMOSs.

We find the gate bias dependence of the noise power of the fabricated electrostatically gated FETs to be consistent with the description of number fluctuation noise with correlated mobility according to Hung et al. [5].

Here we report gate bias referred noise powers down to 1x10⁻⁹V²/Hz for a 20nm wide 10µm long single fin device. The gate bias referred noise PSD reported by Kim et al. [2] is significantly higher (1x10⁻⁸V²/Hz) at 10Hz for a much larger device with an effective width of (50nm+2×40nm)×10 fins and a 10µm length. Converted to the 10µm length and 20nm+2×30nm effective width geometry reported in this work that would amount to ~1.6x10⁻⁹V²/Hz. Rajan et al. [3] report a minimum noise power of ~1x10⁻⁹V²/Hz (already converted to the frequency and 10µm geometry reported in this work).

Fig. 1. Gate voltage referred noise power spectrum showing 1/f noise. A pMOS with 20nm fin width and 1µm channel length is shown. Iᵥ-Vᵥ of the device is shown in the inset (Vᵥ=-0.25V).

Fig. 2. Gate bias dependence of the gate bias referred noise power at 10Hz vs. overdrive for a 20nm wide finfet (gate lengths of 1 and 10µm).

The bias dependence of the noise power determines the bias at which the signal-to-noise ratio (SNR) becomes optimal. The signal-to-noise ratio was investigated in this work for threshold shift signals (as in e.g. ISFETs) by making use of the square rooted inverse gate referred noise power as figure-of-merit for SNR. We find this figure to increase for lower overdrive in contrast to the findings of Rajan et al. [3] who report an optimum at maximum transconductance and in agreement with the findings of Heller et al. [4] for carbon nanotube electrostatically gated FETs.