Low-Frequency Noise Behavior of nMOSFETs with Different Al₂O₃ Capping Layer Thickness and TiN Gate

Danghui Wang  
School of Materials Science and Engineering  
Xi’an Shiyou University  
Xi’an, China  
wdhyxp@163.com

Eddy Simoen, Bogdan Govoreanu,  
Stefan Kubicek, Julien Jussot, B.T. Chan, Nard Dumoulin-Stuyck, Juliana Radu, Dan Mocuta  
Imec  
Leuven, Belgium  
Eddy.Simoen@imec.be

Cor Claeys,  
ESAT  
KU Leuven  
Leuven, Belgium  
cor.claeys@kuleuven.be

Abstract—In this paper, the impact of the thickness of the high-κ Al₂O₃ capping layer on the low-frequency noise performance of nMOSFETs with 8 nm SiO₂ and TiN gate metal has been investigated. It is shown that the predominant 1/f noise is governed by the number fluctuations mechanism. The presence of an Al₂O₃ cap increases the noise Power Spectral Density and, hence, the oxide trap density.

Keywords—Low-frequency noise, Al₂O₃ capping layer, Oxide trap density, TiN gate

I. INTRODUCTION

The threshold voltage (Vth) and the effective work-function of an MOSFET with high-κ/metal gate can be tuned using an appropriate capping layer. Normally, Al₂O₃ is one of the popular capping materials for tuning the Vth of pMOSFETs [1],[2]. At the same time, it has been shown that deposition of a high-κ layer on an SiO₂ interfacial layer increases the effective trap density Ntr [2],[3] and degrades the gate stack reliability [4]. These oxide defects can trap and detraps electrons and holes, which cause number fluctuations of carriers during the transport process in the channel between Source and Drain, giving rise to increased 1/f or flicker noise.

There is currently a strong interest in the implementation of quantum computing on a Complementary Metal-Oxide-Semiconductor (CMOS) platform. Several integration schemes exist, whereby one popular way to define a quantum dot is by electrostatically creating a potential well, using different gates [5]-[7]. This can be achieved by combining metal gates deposited on different gate stacks, corresponding with a different threshold voltage Vth. In the potential well, a quantum bit as information carrier is stored. Such devices are extremely sensitive to the presence of traps in the vicinity of the qubit, so that defect characterization is of high importance for a proper understanding, modeling and optimization of the qubit performance.

In this paper, the impact of the thickness of the high-κ Al₂O₃ capping layer on top of an 8nm SiO₂ gate dielectric of bulk nMOSFETs with TiN metal gate has been investigated using the input characteristics and low-frequency noise. It is shown that the predominant 1/f noise behaves according to the number fluctuations model. The oxide trap density near the SiO₂ interface has been extracted and compared for the different Al₂O₃ capping layer thicknesses using the power spectral density (PSD) of the input-referred voltage noise, showing an increase compared with the cap-free references.

II. EXPERIMENTAL DETAILS

The n-channel devices have been defined by e-beam lithography, with different geometries W×L: 0.1 Pₘ×1 Pₘ; 1 Pₘ×1 Pₘ and 1 Pₘ×10 Pₘ. Three types of gate dielectric stacks, represented schematically in Fig. 1, have been processed, consisting of 8 nm thermal SiO₂; 8 nm SiO₂ + 5 nm Al₂O₃ deposited by Atomic Layer Deposition (ALD) and 8 nm SiO₂ + two times 5 nm Al₂O₃.

According to the input drain current–gate voltage (I_d-V_g) transfer characteristics in linear operation (V_DS=0.05 V), the presence of an Al₂O₃ cap results in a higher threshold voltage Vth. The Vth increases from 0.4 V to 1.4 V (5 nm Al₂O₃) and to 1.55 V (10 nm Al₂O₃) for the 1 Pₘ×10 Pₘ nMOSFETs in Fig. 2.

For noise measurements, the devices were biased in the linear operation region at a drain voltage V_DS=0.05 V and the drain current was stepped from weak to strong inversion, from a drain current of about 10 nA up to 10 Pₜ A.

The input-referred voltage noise Power Spectral Density (PSD) (S_VG) is derived from the measured drain current noise PSD (S_I) by dividing with the transconductance squared (g_m²). As shown in Fig. 3, the obtained noise spectra are predominantly of the 1/f noise type (flicker noise) with γ close to 1.

III. RESULTS AND DISCUSSION

According to Fig. 4, the normalized current noise PSD (S_I/I_d²) at a frequency f=10 Hz exhibits a plateau in weak inversion and a roll off with I_d in strong inversion, for all devices investigated. This strongly suggests that the 1/f noise is due to number fluctuations [8]-[11] and can be
interpreted in terms of trapping/detrapping by defects in the 
SiO$_2$ at a distance between about 1 and 2 nm from the 
interface with the silicon substrate. This is further confirmed 
by the comparison of the normalized noise with $g_m^2/2I_d^2$, in 
Fig. 5.

Fig. 2. Input characteristics corresponding with the reference nMOSFETs 
(upper), the nMOSFETs with 5 nm Al$_2$O$_3$ (middle) and the devices with 
10 nm Al$_2$O$_3$ (lower).

Fig. 3. Low-frequency noise spectra for a 1 $\mu$m x 1 $\mu$m reference 
nMOSFET with 8 nm SiO$_2$, measured at $V_{DS}=0.05$ V and different $I_d$ (10 
nA, 100 nA and 1 $\mu$A).

Fig. 4. Normalized current noise PSD as a function of the drain current in 
linear operation for 1 $\mu$m x 10 $\mu$m nMOSFETs, corresponding with the 
three gate stacks studied.

Fig. 5. Normalized current noise PSD at 10 Hz as a function of the drain 
current in linear operation for 1 $\mu$m x 10 $\mu$m nMOSFETs, corresponding 
with the three gate stacks studied. It is compared with $g_m^2/2I_d^2$ in each case.
For MOSFETs, the number fluctuations 1/f noise PSD can be used to derive the oxide trap density at the interface of the gate stacks. This follows from the correlated mobility fluctuations model, given by [8]-[11]:

\[ S_{VB} = S_{VFB} \left( 1 + \alpha C_{eff} f C_{EOT} \frac{L}{W} \right) \]  

(1a)

with the flat-band voltage noise PSD given by:

\[ S_{VFB} = \frac{q^2 N_{tr}}{W L f C_{EOT} \alpha f} \]  

(1b)

In Eq. (1a), \( \alpha \) is the Coulomb scattering coefficient, \( \mu_{eff} \) the effective low-field mobility, \( W \) is the effective low-field mobility, while in Eq. (1b) \( q \) is the elementary charge, \( kT \) is the thermal energy, \( W \) and \( L \) the effective length and width of the gate, \( f \) is the frequency and \( C_{EOT} \) is the capacitance density corresponding with the Equivalent Oxide Thickness (EOT). The parameter \( \alpha (=1/\kappa) \) is the attenuation factor of the electron wave-function in the gate oxide. If assuming elastic tunneling, one can demonstrate a unique relationship between the trap depth \( z \) and the frequency \( f \), given by [9]-[11]:

\[ z = \alpha^{-1} \ln \left[ 1/\left( 2\pi f \tau_0 \right) \right] \]  

(2)

with \( \tau_0 \) the Shockley-Read-Hall recombination lifetime at the Si/SiO2 interface, for which a typical value of 10^{-10} s is assumed. Thus, a 1/f noise spectrum can be converted into an oxide trap density profile with depth with respect to the Si/SiO2 interface according to Eqs (1)-(2).

Figure 6 compares the \( N_{ot} \) values for the three studied gate stacks at 10 Hz, indicating that the deposition of an \( \text{Al}_2\text{O}_3 \) cap layer results in an increase of \( N_{ot} \). It is also clear that the trap density profile in the SiO2 is rather uniform, which is in line with the frequency exponent close to 1.

Fig. 6. Oxide trap density versus trap depth derived from the flat-band voltage noise PSD for the three gate stacks studied (1 \( \mu \)m \( \times \) 10 \( \mu \)m nMOSFETs).

From the foregoing, it can be concluded that the deposition of an \( \text{Al}_2\text{O}_3 \) layer on top of 8 nm SiO2 leads to a degradation of the oxide quality, due to the increase of the oxide trap density in the vicinity of the Si/SiO2 interface. This is in line with previous observations for Al2O3 cap pMOSFETs [1],[2],[4]. There, it was shown that the deposition of such a Vth shifter yields a roughly one decade increase in \( N_{ot} \), for the case of an SiO2 interfacial oxide with 2 nm HfO2 on top. However, there the traps were aligned with the valence band in silicon. In nMOSFETs, we are probing oxide states close to the silicon conduction band.

One can speculate on the origin of such a degradation of the oxide. It has been for example put forward that the TiN metal gate can cause a gettering of oxygen, creating oxygen vacancy traps [12]-[14]. However, from the result of the reference transistors with a TiN gate on top of SiO2 it can be concluded that this is not the main reason for the oxide trap creation. Indeed, the values found for the trap density in Fig. 6 are typical for good thermal oxide transistors [8]-[11],[15]. Apparently, it is the deposition of the \( \text{Al}_2\text{O}_3 \) layer that leads to a higher \( N_{ot} \) in the gate stacks with a cap layer. This could possibly result from the in-diffusion of Al during ALD, which has been shown to correspond with a higher trap density [1],[2].

IV. CONCLUSIONS

The low-frequency noise of nMOSFETs with 8 nm SiO2 and different \( \text{Al}_2\text{O}_3 \) cap thickness has been investigated. It is shown that the higher 1/f noise PSD found for the capped devices can be ascribed to an increase in the oxide trap density, possibly related with the in-diffusion of Al.

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REFERENCES


