Processing Impact on the Low-Frequency Noise of 1.8 V Input-Output Bulk FinFETs

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Abstract—The low-frequency noise of input-output (I/O) FinFETs is studied for different processing conditions. It is shown that a high-pressure (HP) deuterium (D₂) anneal can improve the noise Power Spectral Density (PSD). In addition, the use of a so-called superlattice architecture is shown to maintain the same gate stack quality.

Keywords—Flicker noise, number fluctuations, oxide trap density

I. INTRODUCTION

System-on-a-Chip (SoC) applications of CMOS technology require the presence of different flavors of transistors. Besides devices for high speed and low power logic, high-voltage Input-Output (I/O) transistors, which are able to operate at higher supply voltage, have to be implemented [1]. The corresponding gate oxide thickness (tOX) is currently in the range of 3 nm, so that standard SiO₂ can serve as a high-reliability gate dielectric for I/O MOSFETs. In order to be compatible with a bulk FinFET process flow, alternatives to standard high-temperature thermal oxidation are being explored.

II. RESULTS AND DISCUSSION

An attractive option in this context could be the Atomic Layer Deposition (ALD) of SiO₂. As shown elsewhere, this yields high-quality and highly reliable I/O transistors [2]. It has also been demonstrated that a high-pressure post-deposition annealing (PDA) or sintering anneal in deuterium (D₂) can improve the interface properties, i.e., the subthreshold slope SS and the density of interface states (Dit) of Si-cap-free SiGe p-channel FinFETs and the overall device performance [3]. Further along the roadmap, vertically stacked horizontal gate-all-around nanowire FETs are promising candidates because they allow a more aggressive gate length scaling [4]. However, the spacing between stacked nanowire devices does not accommodate the thick oxide for I/O FETs. Alternatively, one can consider a Si/SiGe/Si/SiGe/Si superlattice FinFET for I/O applications. It is the goal of the present work to report on the low-frequency noise behavior of these different types of I/O FinFETs. For example, it is shown in Fig. 1 that the average flat-band voltage noise Power Spectral Density (PSD) at 10 Hz can be improved by application of a High-Pressure (HP) D₂ anneal. At the same time, Fig. 2 illustrates that the noise of the superlattice FinFET is not compromised compared with the reference device architecture.

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